

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1–16 (canceled)

Claim 17 (new). A clock signal extraction device for extracting an extracted clock signal out of a periodic data signal, comprising:

- a first clock generator circuit configured to generate a rising edge clock signal, the first clock generator circuit having a first output;
- a first phase detector configured to detect a first phase difference between a rising edge of the periodic data signal and a rising edge of the rising edge clock signal, the first phase detector having a first input connected to the first output to form a first loop, and wherein the first clock generator circuit and the first phase detector cooperate to reduce the detected first phase difference,
- a second clock generator circuit configured to generate a falling edge clock signal, the second clock generator circuit having a second output;
- a second phase detector configured to detect a second phase difference between a falling edge of the data signal and a falling edge of the falling edge clock signal, the second phase generator having a second input connected to the second output to form a second loop, and wherein the second clock generator circuit and the second phase detector cooperate to reduce the detected second phase difference;

- a third clock generator circuit configured to generate the extracted clock signal based on an average of the first phase difference and the second phase difference such that the probability distribution functions of the rising edges and falling edges of the periodic data signal are individually averaged.

Claim 18 (new). The clock signal extraction device according to claim 17, wherein the third clock generator circuit includes a controller and a third clock generator, the controller configured to process said first phase difference and said second phase difference to control generation of the extracted clock signal by the third clock generator.

Claim 19 (new). The clock signal extraction device according to claim 18, wherein the controller further constitutes a part of the first clock generator circuit and the second clock generator circuit.

Claim 20 (new). The clock signal extraction device according to claim 19, wherein each of said first, second and third clock generator circuits includes a voltage controlled oscillator.

Claim 21 (new). The clock signal extraction device according to claim 17, wherein each of said first, second and third clock generator circuits includes a voltage controlled oscillator.

Claim 22 (new). The clock signal extraction device according to claim 17, wherein each of the first, second and third clock generator circuits includes a phase pump and a loop filter.

Claim 23 (new). The clock signal extraction device according to claim 19, wherein the controller further comprises, for each of the first, second and third clock generator circuits, a phase pump and a loop filter.

Claim 24 (new). An arrangement for extracting data, including:

- a clock signal extraction device for extracting an extracted clock signal out of a periodic data signal, comprising

- a first clock generator circuit configured to generate a rising edge clock signal, the first clock generator circuit having a first output,

- a first phase detector configured to detect a first phase difference between a rising edge of the periodic data signal and a rising edge of the rising edge clock signal, the first phase detector having a first input connected to the first output to form a first loop, and wherein the first clock generator circuit and the first phase detector cooperate to reduce the detected first phase difference,

- a second clock generator circuit configured to generate a falling edge clock signal, the second clock generator circuit having a second output;

- a second phase detector configured to detect a second phase difference between a falling edge of the data signal and a falling edge of the falling edge clock signal, the second phase generator having a second input connected to the second output

to form a second loop, and wherein the second clock generator circuit and the second phase detector cooperate to reduce the detected second phase difference,

a third clock generator circuit configured to generate the extracted clock signal based on an average of the first phase difference and the second phase difference such that the probability distribution functions of the rising edges and falling edges of the periodic data signal are individually averaged; and

a data extraction device configured to extract data from said data signal according to a rate of said extracted clock signal.

Claim 25. The arrangement according to claim 24, wherein the third clock generator circuit includes a controller and a third clock generator, the controller configured to process said first phase difference and said second phase difference to control generation of the extracted clock signal by the third clock generator.

Claim 26 (new). The arrangement according to claim 25, wherein said controller controls said third clock generator to generate said clock signal such that the error rate of the extracted data is minimized.

Claim 27 (new). The arrangement according to claim 24, wherein said data extraction device comprises a data sampler for sampling said data signal.

Claim 28 (new). The arrangement according to claim 27, wherein said data sampler comprises a D-type flip-flop.

Claim 29 (new). A method for extracting an extracted clock signal out of a periodic data signal, comprising:

- (a1) generating a rising edge clock signal;
- (a2) detecting a first phase difference between a rising edge of the periodic data signal and a rising edge of a rising edge clock signal;
- (a3) feeding back the first phase difference to generate a subsequent rising edge clock signal having a reduced first phase difference;
- (b1) generating a falling edge clock signal;
- (b2) detecting a second phase difference between a falling edge of the periodic data signal and a falling edge of a falling edge clock signal;
- (b3) feeding back the second phase difference to generate a subsequent falling edge clock signal having a reduced second phase difference; and
- (c) generating the extracted clock signal based on an average of a plurality of first phase differences and second phase differences in a way that the probability distribution functions of the rising edges and falling edges of the periodic data signal are individually averaged.

Claim 30 (new). The method according to claim 29, where step (a1) includes employing a voltage controlled oscillator to generate the first clock signal and the subsequent first clock signal.

Claim 31 (new). The method according to claim 30, where step (a2) includes employing a voltage controlled oscillator to generate the second clock signal and the subsequent second clock signal.

Claim 32 (new). The method according to claim 29, further comprising a step of:

- extracting data from said data signal according to a rate of said extracted clock signal.

Claim 33 (new). The method according to claim 32, wherein step c) further comprises generating the extracted clock signal such that the error rate of said extracted data is minimized.

Claim 34 (new). The method according to claim 33, wherein said data signal is an optical data signal.

Claim 35 (new). The method according to claim 33, further comprising extracting data from said data signal using a flip-flop.

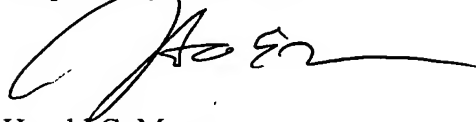
Claim 36 (new). The method according to claim 29, wherein said data signal is an optical data signal.

II. Conclusion

Applicants respectfully request entry of the amendment and favorable consideration of the application.

A prompt and favorable action on the merits is requested.

Respectfully Submitted,

A handwritten signature in black ink, appearing to read 'H. C. Moore', with a long horizontal flourish extending to the right.

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